

App No. 10/750 960

Sheet 1 of 4

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.

58268.00366

SERIAL NO.

New Continuation

LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

APPLICANT

Dennis Sungik LEE et al.

FILING DATE

January 6, 2003

GROUP

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DD	AA	5,555,398	Sep. 1996	Raman			
	AB	5,644,784	Jul. 1997	Peek			
	AD	5,828,653	Oct. 1998	Goss			
	AE	5,423,015	Jun. 1995	Chung			
	AF	5,696,899	Dec. 1997	Kalwitz			
	AG	6,061,351	May 2000	Erimli et al.			
	AH	5,748,631	May 1998	Bergantino et al.			
	AI	6,119,196	Sep. 2000	Muller et al.			
	AJ	6,175,902 B1	Jan. 2001	Runaldue et al.			
	AK	5,473,607	Dec. 1995	Hausman et al.			
	AL	5,787,084	Jul. 1998	Hoang et al.			
	AM	5,845,081	Dec. 1998	Rangarajan et al.			
	AN	5,892,922	Apr. 1999	Lorenz			
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	AV	6,041,053	Mar. 2000	Douceur et al.			
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	AX	5,909,686	Jun. 1999	Muller et al.			
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	BI	5,842,038	Nov. 1998	Williams et al.			
	BJ	5,742,613	Apr. 1998	MacDonald			
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	BO	5,983,223	Nov. 1999	Perlmann			
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	BU	EP0859492A2	Aug. 1998	EPO					
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	BW	EP0853441A2	Jul. 1998	EPO					
	BX	4-189023	Jul. 1992	Japan					Abs
	BY	WO 98/09473	Mar. 1998	WIPO					
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	CB	FR 2 725 573 - A1	Apr. 1996	France					Abs
	CD	EP0854606A2	Jul. 1998	EPO					
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CN	"A High-Speed CMOS Circuit for 1.2-Gb/s 16 x 16 ATM Switching," Alain Chemarin et al. 8107 IEEE Journal of Solid-State Circuits 27(1992) July, No. 7, New York, US, pages 1116-1120
CO	"Local Area Network Switch Frame Lookup Technique for Increased Speed and Flexibility," 700 IBM Technical Disclosure Bulletin 38(1995) July, No. 7, Armonk, NY, US, pages 221-222
CP	"Queue Management for Shared Buffer and Shared Multi-buffer ATM Switches," Yu-Sheng Lin et al., Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, R.O.C., March 24, 1996, pages 688-695
CQ	"A 622-Mb/s 8 x 8 ATM Switch Chip Set with Shared Multibuffer Architecture," Harufusa Kondoh et al., 8107 IEEE Journal of Solid-State Circuits 28(1993) July, No. 7, New York, US, pages 808-814
CR	"Catalyst 8500 CSR Architecture," White Paper XP-002151999, Cisco Systems Inc. 1998, pages 1-19
CS	"Computer Networks," A.S. Tanenbaum, PRENTICE-HALL INT., USA, XP-002147300(1998), Sec. 5.2- Sec. 5.3, pages 309-320
CT	Kenneth Schultz, et al., "Architectures for Large-Capacity CAMs," Integration, the VLSI Journal, North Holland Publishing Company, Amsterdam, The Netherlands, vol. 18, no. 2, 1 June 1995
CU	Elm et al., "Functional Memory Array Testing Using Associative Search Algorithms," European Test Conference, 1993, Proceedings to ETC 93, Third, 19-22 April 1993, pp. 139-148



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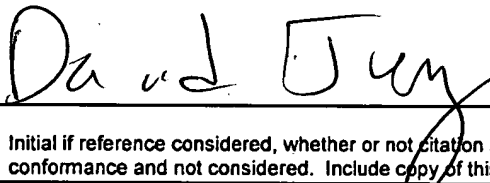
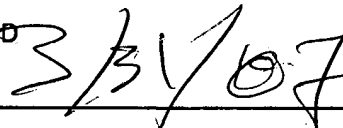
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FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 58268.00366	SERIAL NO. New Continuation
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	CV	Pao et al., "Efficient Hardware Architecture for Fast IP Address Lookup," INFOCOM 2002, Twenty-First Annual Joint Conference of the IEEE Computer and Communication Societies, Proceedings, IEEE Vol. 2, 23-27 June 2002, pp 555-561, vol. 2
	CW	Eim et al., "Fault Detection and Fault Localization Using IDDQ-Testing in Parallel Testable FAST-SRAMs," VLSI Test Symposium, 1994, Proceedings, 12th IEEE, 25-28 April 1994, pp 380-385

EXAMINER		DATE CONSIDERED	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			